REMARKS

The Examiner rejected claims 1-11 under 35 U.S.C. §102(b) as being unpatentable over Parris et al. (US 5,929,478).

Applicants respectfully traverse the §102(b) rejections with the following arguments.

35 USC § 102

As to claim 3, the Examiner states "the structure includes a third horizontal Layer 32 (fig. 3) of said second dopant type (col. 4, lines 5-8) on top of and in contact with said first Layer 22 (fig. 3) and extending vertically into said first Layer 22 (fig. 3), said second Layer 27 (fig. 3) further electrically modulated by said third Layer 32 (fig. 3)."

Applicants contend that claim 3, as amended, is not anticipated by Parris et al. because Parris et al does not teach each and every feature of claim 3. For example, Parris et al. does not teach "a third semiconductor layer of said second dopant type a bottom surface of said third semiconductor layer in direct physical contact with said top surface of said first semiconductor layer and extending in a direction perpendicular to said top surface of said substrate into said second semiconductor layer, said second layer further electrically modulated by said third semiconductor layer."

Applicants respectfully point out that field oxide 32 of Parris et al. is not a semiconductor layer, but rather an oxide layer and further, the oxide layer 32 is not doped. Col. 3, lines 13-17 of Parris et al. states " Isolation structures such as, for example, field oxide regions 32 are formed over epitaxial layer 22 using techniques well known to those skilled in the art. Preferably, ion implantation is performed **before** forming field oxide regions 32 to form doped regions (not shown) under field oxide regions 32." Col. 4, lines 5-9 of Parris et al states " Ions of N conductivity type, e. g., phosphorous or arsenic ions, are implanted through openings in a masking layer (not shown) **and** in field oxide regions 32 into epitaxial layer 22 to form a source region 41 and a drain region 42 of FET 11 in well 27." Thus, the Examiners "layer 32" of Parris et al. is not a semiconductor layer and is not doped.

Based on the preceding arguments, Applicants respectfully maintain that claim 3 is not unpatentable over Parris et al. and is in condition for allowance. Since claims 4-11 depend from claim 3, Applicants respectfully maintain that claims 4-11 are likewise in condition for allowance.

As to claim 4, the Examiner states "the third Layer 32 (fig. 3) extends horizontally under said source 41 (fig. 3), said drain 42 (fig. 3) and said gate 36 (fig. 3)."

Applicants contend that claim 4, as amended, is not anticipated by Parris et al. because Parris et al does not teach each and every feature of claim 4. For example, Parris et al. does not teach "wherein said third semiconductor layer extends parallel to said top surface of said substrate in said second semiconductor layer between said source, said drain and said gate and said first semiconductor layer.

Applicants respectfully point out that in FIG. 3 of Parris et al. while field oxide 32 abuts drain 42, it does not extend " parallel to said top surface of said substrate in said second semiconductor layer between said source, said drain and said gate and said first semiconductor layer" as Applicants claim 4 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 4 is not unpatentable over Parris et al. and is in condition for allowance.

As to claim 5, the Examiner states "the third Layer 32 (fig. 3) extends horizontally under a shallow trench isolation 49, or 62 (fig. 3) formed between said source 41 (fig. 3)or said drain 42 (fig. 3) and a contact to said second Layer 27 (fig. 3)."

Applicants contend that claim 5, as amended, is not anticipated by Parris et al. because Parris et al does not teach each and every feature of claim 5. For example, Parris et al. does not teach "wherein said third semiconductor layer extends parallel to said top surface of said

substrate in said second semiconductor layer between said second semiconductor layer and said shallow trench dielectric isolation."

Applicants respectfully point out the Examiner has failed state which element of FIG. 3, the Examiner deems is the contact to said second layer so Applicants are not able to fully reply to the Examiners rejection of claim 5.

First, Applicants respectfully point out that element 49 is not shallow trench dielectric isolation but a substrate contact (highly doped region) of semiconductor well 51 and that element 62 is not shallow trench dielectric isolation but a contact (highly doped region) to epitaxial layer 22. Second, third layer 32 does not extend parallel to the top surface of substrate 21 in second layer 27 between second layer 27 and alleged shallow trench isolation 49.

Based on the preceding arguments, Applicants respectfully maintain that claim 5 is not unpatentable over Parris et al. and is in condition for allowance.

As to claim 6, the Examiner states "the third Layer 32 (fig. 3) extends horizontally under a contact 58 (fig. 3) to said second Layer 27 (fig. 3)."

Applicants contend that claim 6, is not anticipated by Parris et al. because Parris et al does not teach each and every feature of claim 6. For example, Parris et al. does not teach "wherein said third semiconductor layer extends parallel to said top surface of said substrate in said second semiconductor layer between said contact to said second semiconductor layer and said first semiconductor layer." Applicants point out that third layer 32 does not extends parallel to the top surface of substrate 21 in the second layer 51 between contact 58 to said second layer 51 and first layer 22.

Based on the preceding arguments, Applicants respectfully maintain that claim 6 is not unpatentable over Parris et al. and is in condition for allowance.

As to claim 7, the Examiner states "a vertical isolation 58 (fig. 3) comprising shallow trench isolation 49 (fig. 3) in combination with deep trench isolation 29 (fig. 3), said vertical isolation 58 (fig. 3) extending vertically from said top surface of said substrate 21 (fig. 3) into or past said first Layer 22 (fig. 3) and isolating said second Layer 27 (fig. 3)."

First, Applicants respectfully point out that element 49 is not shallow trench dielectric isolation but a substrate contact (highly doped region) of semiconductor well 51 and that element 29 is not deep trench dielectric isolation but a diffused (highly doped region) of semiconductor material. Second, Applicants fail to see how element 58 can be comprised of element 49 in combination with element 29. Element 58 is a distinct element. Third, element 58 does extend into first layer 22.

Based on the preceding arguments, Applicants respectfully maintain that claim 7 is not unpatentable over Parris et al. and is in condition for allowance.

As to claim 9, the Examiner states "the first horizontal Layer 22 (fig. 3) is the same as a subcollector of a bipolar transistor 11 (fig. 3) formed in said substrate 21 (fig. 3)."

Applicants contend that claim 9, as amended, is not anticipated by Parris et al. because Parris et al does not teach each and every feature of claim 96. For example, Parris et al. does not teach "said third semiconductor layer comprises a collector of a bipolar transistor and said first semiconductor layer comprises a subcollector of said bipolar transistor formed in said substrate."

Applicants believe in claim 1, that the Examiner suggests that bipolar transistor 11 comprises an emitter (source 41), a base (second layer 27) and a subcollector (first layer 22). However layer 32 can function as either a collector, because it is not semiconductor material and because it is located in a position making it impossible to function as a collector.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Voldman et al.

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